a dual damascene structure adjacent the second metal feature and having a damascene trench portion extending through the second interlevel dielectric layer and the second etch stop layer and terminating at the first interlevel dielectric layer and further including a damascene via portion C2 extending through the first interlevel dielectric layer and the first etch stop layer and connecting the trench portion to the first metal feature.

30. (New) The semiconductor device as recited in Claim 29 wherein the unsegmented via is a passing metal via with no passing metal feature.--

REMARKS

The Applicant has carefully considered this application in connection with the Examiner's Action and respectfully requests reconsideration of this application in view of the foregoing amendment and the following remarks. The Applicant originally filed Claims 1-28. Pursuant to a restriction requirement, Claims 1-20 were previously withdrawn without prejudice or disclaimer. Claims 22, 23 and 26 were also previously canceled without prejudice or disclaimer. The Applicant presently amends Claims 21 and adds new Claims 29-30. Accordingly, Claims 21, 24, 25 and 27-30 are currently pending in the present application.

I. Formal Matters

The Examiner has objected to the drawings, asserting that the drawings fail to show some elements of Claims 25 and 27. While the Applicant does not necessarily agree with the Examiner's objections, the Applicant has amended the drawings to more clearly illustrate an embodiment of the

invention recited in the claims and described in the specification. Accordingly, a Proposed Drawing Amendment is submitted herewith. Consequently, the Applicant requests the Examiner withdraw the objection to the drawings.

II. Rejection of Claims 21, 24 and 25 under 35 U.S.C. §102

The Examiner has rejected Claims 21, 24 and 25 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,163,067 to Inohara, *et al.* ("Inohara"). However, Inohara fails to anticipate independent Claim 21 and its dependent Claims 24 and 25 because Inohara fails to disclose each and every element of Claim 21. Specifically, Inohara fails to disclose a third interconnect metal located on or in a third interlevel dielectric layer, the third interlevel dielectric layer located over a second dielectric layer, as recited in Claim 21. In contrast, Inohara merely discloses a first interconnect metal collectively formed by underlayer films 16a and conductor members 16b (as illustrated in FIGs. 12-14), and briefly discusses a second interconnect metal of the prior art formed by a conductor film 20 (as illustrated in FIG. 3 and described at column 1, lines 62-66), but fails to suggest or even mention the possibility of a third interconnect metal located on or in a third interlevel dielectric layer, the third interlevel dielectric layer located over a second dielectric layer. Moreover, because Inohara fails to disclose such a third interconnect metal, Inohara fails to disclose a via connecting a third interconnect metal to the underlayer films 16a or conductor members 16b discussed above.

Accordingly, Inohara fails to disclose each and every element recited in Claim 21. Therefore, Inohara is not an anticipating reference with respect to Claim 21 and its dependent Claims 24 and

25. Consequently, the Applicant requests the Examiner withdraw the §102 rejection with respect to Claims 21, 24 and 25.

Inohara also fails to anticipate new Claims 29 and 30 because Inohara fails to disclose a first metal feature connected to both an unsegmented via and a damascene via portion as recited in Claim 29, and because Claim 30 is dependent on Claim 29. In contrast, the Examiner asserts that one of the salicide layers 25 disclosed in Inohara is a first metal feature connected to both an unsegmented via and a damascene via portion. In support thereof, the Examiner asserts that the contact hole 32 shown on the right side of Inohara's FIGs. 12 and 14 is an unsegmented via, and that the conducting member 16c shown on the left side of Inohara's FIGs. 12-14 is a damascene via portion (as best understood by the Applicant). However, withholding comment on the accuracy of the Examiner's assertions regarding such an unsegmented via and damascene via portion, these two elements do not connect to a mutual metal feature. In contrast, the Examiner's asserted unsegmented via connects to a salicide layer 25 embedded in a drain region 22b or the drain region 22b itself, and the Examiner's asserted damascene via portion connects to another separate and distinct salicide layer 25 embedded in a source region 22a or the source region 22a itself, as shown in FIGs. 12 and 13. Inohara fails to disclose that the multiple salicide layers 25 shown in FIG. 13 are the same metal feature, or are even interconnected. In fact, as shown in FIG. 13, the multiple salicide layers 25 are isolated from each other by a field oxide layer 12 and a stopper film 13a. Moreover, in the embodiments in which the Examiner's asserted unsegmented via connects directly to the drain region 22b, and the Examiner's asserted damascene via portion connects directly to the source region 22a, one skilled in the art would not be motivated to connected the Examiner's asserted unsegmented via

and damascene via portion to the same metal feature, because such a connection would short circuit the source and drain regions 22a, 22b, rendering the device useless.

Accordingly, Inohara fails to disclose a first metal feature connected to both an unsegmented via and a damascene via portion, as recited in Claim 29. Therefore, Inohara is not an anticipating reference with respect to Claim 29 and its dependent Claim 30.

III. Rejection of Claims 27 and 28 under 35 U.S.C. §103

The Examiner has rejected Claims 27 and 28 under 35 U.S.C. §103 as being unpatentable over Inohara in view of U.S. Patent No. 6,127,260 to Huang, *et al.* ("Huang"). However, as discussed above, Inohara fails to teach a third interconnect metal located on or in a third interlevel dielectric layer, the third interlevel dielectric layer located over a second dielectric layer, and a via connecting the third interconnect metal to a first interconnect metal, as recited in Claim 21, among other elements. Moreover, Inohara fails to suggest such a third interconnect metal and connecting via because, as discussed above, Inohara provides no teaching, suggestion, motivation or even mere mention of providing a third interconnect metal, especially one that is connected to a first interconnect metal by a via through second and third interlevel dielectric layers, as recited in Claim 21.

In addition, Huang adds nothing to Inohara, because Huang also fails to teach or suggest a third interconnect metal located on or in a third interlevel dielectric layer, the third interlevel dielectric layer located over a second dielectric layer, and a via connecting the third interconnect metal to a first interconnect metal wherein the via is void of a landing pad, as recited in Claim 21, among other elements. In contrast, Huang merely teaches first interconnect metal structures 51, 52

overlaying and contacting a top surface of upper metal plug structures, and fails to provide any suggestion, motivation or mere mention of second and third interconnect metals or a via connecting a third interconnect metal to the interconnect metal structures 51, 52.

Accordingly, the combination of Inohara and Huang fails to teach or suggest each and every element recited in Claim 21. The combination therefore fails to support a *prima facie* case of obviousness of Claim 21 and its dependent Claims 27 and 28. Consequently, the Applicant requests the Examiner withdraw the §103 rejection with respect to Claims 27 and 28.

The combination of Inohara and Huang also fails to support a *prima facie* case of obviousness of new Claims 29 and 30 because the combination fails to teach or suggest a first metal feature connected to both an unsegmented via and a damascene via portion as recited in Claim 29, and because Claim 30 is dependent on Claim 29. Inohara fails to teach or suggest a first metal feature connected to both an unsegmented via and a damascene via portion. In addition, Huang adds nothing to Inohara, because Huang also fails to teach or suggest a first metal feature connected to both an unsegmented via and a damascene via portion. In fact, Huang fails to even mention a damascene via portion, or any damascene structure whatsoever. In contrast, Huang discloses a metal plug structure in a narrow diameter contact hole, the structure comprising an upper level metal plug structure in a top portion of the narrow diameter contact hole, the upper level metal plug structure overlying and contacting a tee shaped lower level metal plug structure in a bottom portion of the narrow diameter contact hole. (Column 3, lines 26-31).

Accordingly, the combination of Inohara and Huang fails to teach or suggest a first metal feature connected to both an unsegmented via and a damascene via portion, as recited in Claim 29. Therefore, the combination of Inohara and Huang fails to teach or suggest each and every element

of Claim 29 and its dependent Claim 30. The combination therefore fails to support a *prima facie* case of obviousness of new Claims 29 and 30.

IV. Rejection of Claims 21 and 24 under 35 U.S.C. §103

The Examiner has rejected Claims 21 and 24 under 35 U.S.C. §103 as being unpatentable over U.S. Patent No. 6,225,207 to Parikh. However, Parikh fails to teach or suggest a third interconnect metal located on or in a third interlevel dielectric layer, the third interlevel dielectric layer located over a second dielectric layer, and a via connecting the third interconnect metal to a first interconnect metal, as recited in Claim 21. In contrast, Parikh teaches a first interconnect metal comprising power lines 650, 658 and a second interconnect metal comprising signal lines 654, 660, as shown in FIG. 6B, and fails to provide any suggestion, motivation or even mere mention of an additional interconnect metal as recited in Claim 21 of the present application. Moreover, because Parikh fails to teach or suggest such a third interconnect metal, Parikh fails to disclose a via connecting a third interconnect metal to the power lines 650, 658 signal lines 654, 660 discussed above.

Accordingly, Parikh fails to teach or suggest each and every element recited in Claim 21. Therefore, Parikh fails to support a *prima facie* case of obviousness of Claim 21 and its dependent Clam 24. Consequently, the Applicant requests the Examiner withdraw the §103 rejection with respect to Claims 21 and 24.

Parikh also fails to support a *prima facie* case of obviousness of new Claims 29 and 30 because Parikh fails to teach or suggest a first metal feature connected to both an unsegmented via and a damascene via portion as recited in Claim 29, and because Claim 30 is dependent on Claim

29. In contrast, Parikh merely discloses that the signal line via plug 656 and the power line via plug 652 connect to a semiconductor substrate 610, as shown in Parikh's FIG. 6B (column 12, lines 17-20), and that the semiconductor substrate 610 includes structures and devices comprising typical IC elements, components, interconnects and semiconductor materials (column 6, lines 63-66). Those skilled in the art understand that such a semiconductor substrate is not a metal feature. Moreover, Parikh discloses that the signal line via plug 656 carries IC signals, and that the power line via plug 652 carries power. (Column 6, lines 49-51). Those skilled in the art also understand that metal features carrying IC signals are not connected to metal features carrying power, which further reinforces that the signal line via plug 656 and power line via plug 652 are not connected to the same metal feature.

Accordingly, Parikh fails to teach or suggest a first metal feature connected to both an unsegmented via and a damascene via portion, as recited in Claim 29. Therefore, Parikh fails to teach or suggest each and every element of Claim 29 and its dependent Claim 30. Parikh therefore fails to support a *prima facie* case of obviousness of Claims 29 and 30.

V. Rejection of Claims 25, 27 and 28 under 35 U.S.C. §103

The Examiner has rejected Claims 25, 27 and 28 under 35 U.S.C. §103 as being unpatentable over Parikh in view of Huang. However, as discussed above, Parikh and Huang independently fail to teach or suggest a third interconnect metal located on or in a third interlevel dielectric layer, the third interlevel dielectric layer located over a second dielectric layer, and a via connecting the third interconnect metal to a first interconnect metal, as recited in Claim 21. Therefore, the combination of Parikh and Huang fails to teach or suggest each and every element of Claim 21 and its dependent

Claims 25, 27 and 28. The combination therefore fails to support a *prima facie* case of obviousness of Claims 25, 27 and 28. Consequently, the Applicant requests the Examiner withdraw the §103 rejection with respect to Claims 25, 27 and 28.

The combination of Parikh and Huang also fails to support a *prima facie* case of obviousness of new Claims 29 and 30 because, as discussed above, the combination fails to teach or suggest a first metal feature connected to both an unsegmented via and a damascene via portion, as recited in Claim 29, and because Claim 30 is dependent on Claim 29.

VI. Conclusion

In view of the foregoing amendment and remarks, the Applicant now sees all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicits a Notice of Allowance for Claims 21, 24, 25 and 27-30.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned **"Version with markings to show changes made."**

The Applicant requests the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

(1) Please amend Claim 21 as follows:

21. (Three Times Amended) A semiconductor device, comprising:

[a first metal feature located over a semiconductor surface and having a first etch stop layer and a first interlevel dielectric layer located thereover and a second etch stop layer and a second interlevel dielectric layer located over the first etch stop layer and the first interlevel dielectric layer;

an unsegmented via located through the first and second etch stop layers and interlevel dielectric layers, the via extending to and contacting the first metal feature, the via being void of a landing pad between the first and second interlevel dielectric layers;

a second metal feature located adjacent the unsegmented via and extending through the second interlevel dielectric layer and the second etch stop layer and terminating at the first interlevel dielectric layer; and

a dual damascene structure adjacent the second metal feature and having a damascene trench portion extending through the second interlevel dielectric layer and the second etch stop layer and terminating at the first interlevel dielectric layer and further including a damascene via portion extending through the first interlevel dielectric layer and the first etch stop layer and connecting the trench portion to the first metal feature]

a first interconnect metal located on or in a first interlevel dielectric layer;

a second interconnect metal located on or in a second interlevel dielectric layer, the second interlevel dielectric layer located over the first interlevel dielectric layer;

a third interconnect metal located on or in a third interlevel dielectric layer, the third interlevel dielectric layer located over the second dielectric layer; and

a via located through the second and third interlevel dielectric layers and connecting the first and third interconnect metals, the via being void of a landing pad between the second and third interlevel dielectric layers.

(2) Please add the following new Claims 29-30 as follows:

–29. (New) A semiconductor device, comprising:

a first metal feature located on a semiconductor surface;

a first etch stop layer located on the first metal feature;

a first interlevel dielectric layer located on the first etch stop layer;

a second etch stop layer located on the first interlevel dielectric layer;

a second interlevel dielectric layer located on the second etch stop layer;

an unsegmented via located through the first and second etch stop layers and interlevel dielectric layers, the unsegmented via extending to and contacting the first metal feature and being void of a landing pad between the first and second interlevel dielectric layers;

a second metal feature located adjacent the unsegmented via and extending through the second interlevel dielectric layer and the second etch stop layer and terminating at the first interlevel dielectric layer; and

a dual damascene structure adjacent the second metal feature and having a damascene trench portion extending through the second interlevel dielectric layer and the second etch stop layer and terminating at the first interlevel dielectric layer and further including a damascene via portion extending through the first interlevel dielectric layer and the first etch stop layer and connecting the trench portion to the first metal feature.

30. (New) The semiconductor device as recited in Claim 29 wherein the unsegmented via is a passing metal via with no passing metal feature.--